



FAST CMOS 16-BIT BUS TRANSCEIVER/REGISTER

IDT74FCT16652AT/CT

FEATURES:

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- $V_{CC} = 5V \pm 10\%$
- High drive outputs (-32mA I_{OH} , 64mA I_{OL})
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

DESCRIPTION:

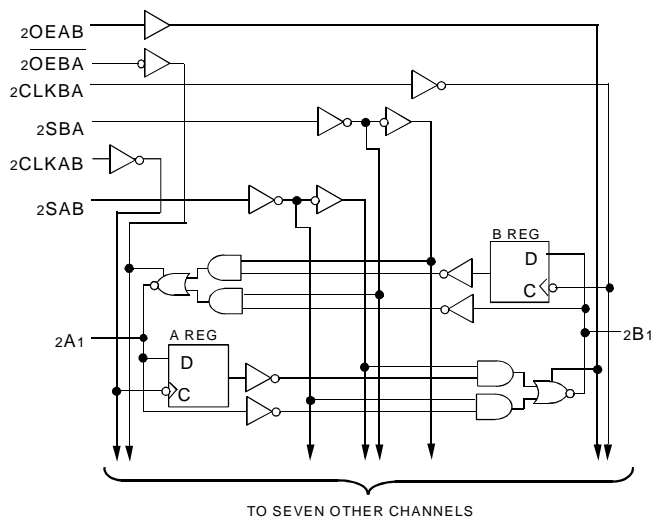
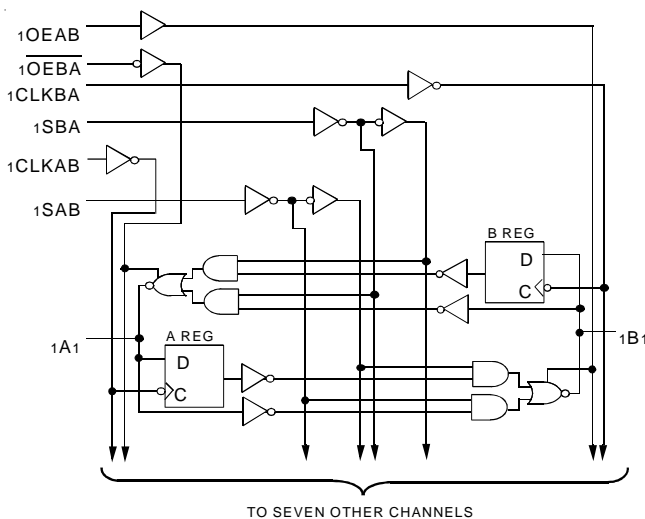
The FCT16652T 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. For example, the $xOEAB$ and $xOEBA$ signals control the transceiver functions.

The $xSAB$ and $xSBA$ control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A low input level selects real-time data and a high level selects stored data.

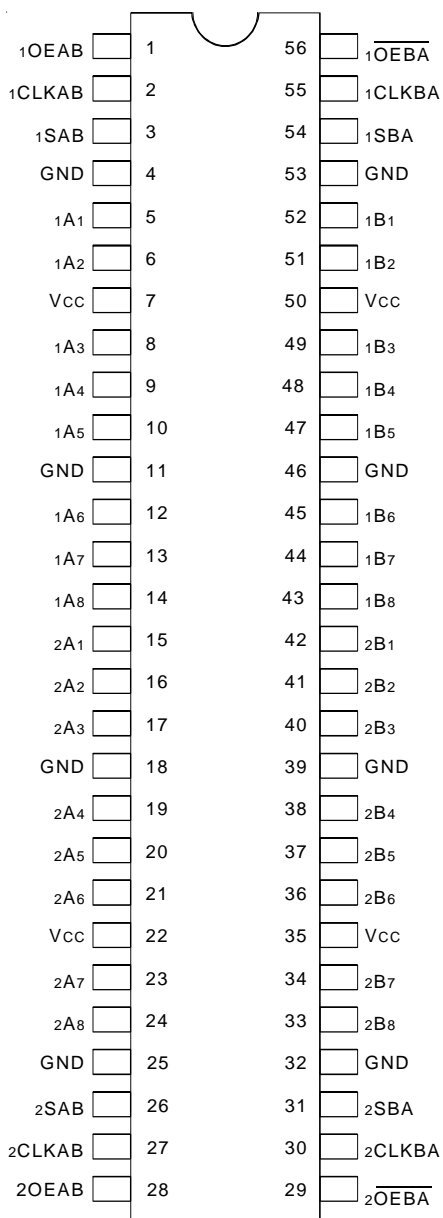
Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by low-to-high transitions at the appropriate clock pins ($xCLKAB$ or $xCLKBA$), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16652T is ideally suited for driving high capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

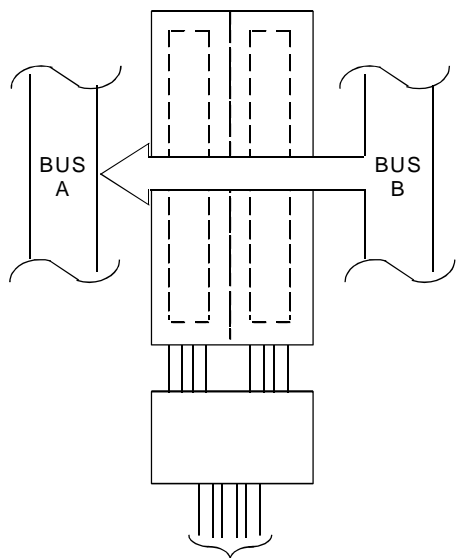
Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, xOEBA	Output Enable Inputs

FUNCTION TABLE

Inputs						Data I/O ⁽¹⁾		Operation or Function
xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾	Store A, Hold B
H	H	↑	↑	X ⁽²⁾	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified ⁽¹⁾	Input	Hold A, Store B
L	L	↑	↑	X	X ⁽²⁾	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

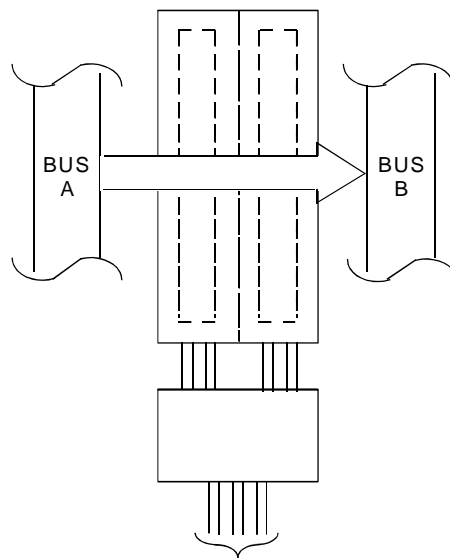
NOTES:

- The data output functions may be enabled or disabled by various signals at the xOEAB or $\overline{\text{xOEBA}}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clocks inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care
↑ = LOW-to-HIGH Transition



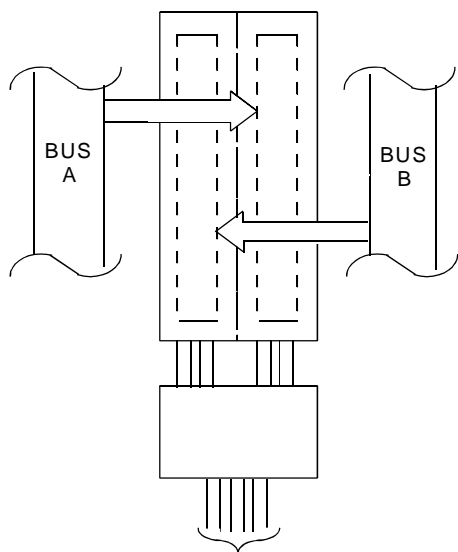
xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

*Real-Time Transfer
Bus B to A*



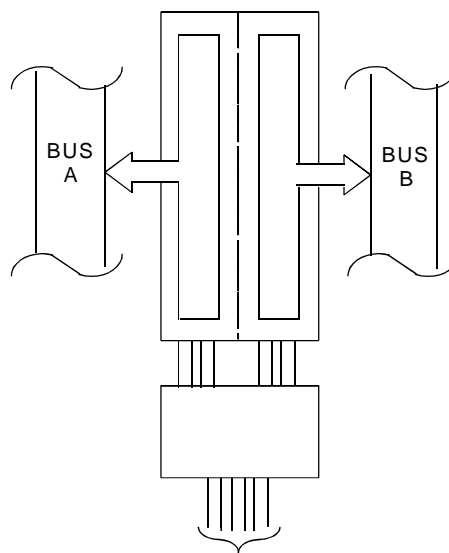
xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

*Real-Time Transfer
Bus A to B*



xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

*Storage from
A and/or B*



xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

*Transfer Stored
Data to A and/or B*

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_i = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_o = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL}	Quiescent Power Supply Current	$V_{CC} = \text{Max}$		—	5	500	μA
I_{CCH}		$V_{IN} = \text{GND or } V_{CC}$					
I_{CCZ}							

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_O	Output Drive Current	$V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$		-50	—	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA}$	2.4	3.5	—	
			$I_{OH} = -32\text{mA}^{(4)}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_o \leq 4.5\text{V}$		—	—	± 1	μA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. This test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open xOEAB = xOEBA = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz (xCLKBA) 50% Duty Cycle xOEAB = xOEBA = GND One Bit Toggling f _i = 5MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.8	1.7	mA
			V _{IN} = 3.4V V _{IN} = GND	—	1.3	3.2	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz (xCLKBA) 50% Duty Cycle xOEAB = xOEBA = GND Sixteen Bits Toggling f _i = 2.5MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	3.8	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	8.3	20 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i

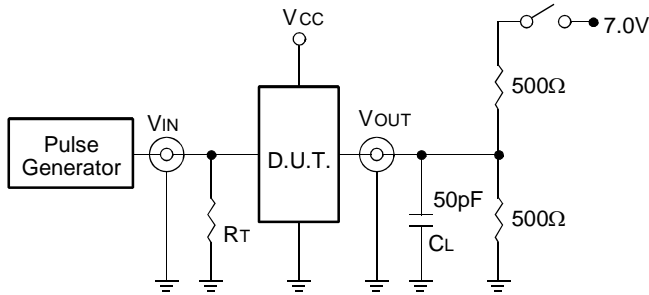
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	74FCT16652AT		74FCT16652CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	C _L = 50pF R _L = 500Ω	2	6.3	1.5	3.9	ns
t _{PZH} t _{PZL}	Output Enable Time xOEAB or xOEBA to Bus		2	9.8	1.5	4.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time xOEAB or xOEBA to Bus		2	6.3	1.5	4.4	ns
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus		2	6.3	1.5	4.1	ns
t _{PLH} t _{PHL}	Propagation Delay xSBA or xSAB to Bus		2	7.7	1.5	4.2	ns
t _{SU}	Set-Up Time, HIGH or LOW Bus to Clock		2	—	2	—	ns
t _H	Hold Time, HIGH or LOW Bus to Clock		1.5	—	0	—	ns
t _W	Clock Pulse Width, HIGH or LOW		5	—	3	—	ns
t _{SK(0)}	Output Skew ⁽³⁾		—	0.5	—	0.5	ns

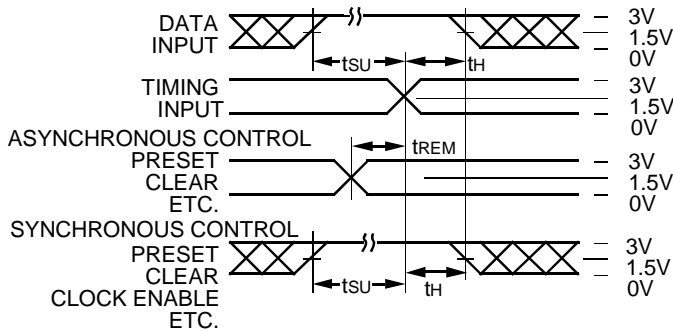
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

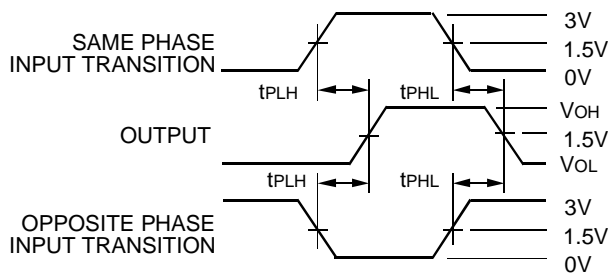
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

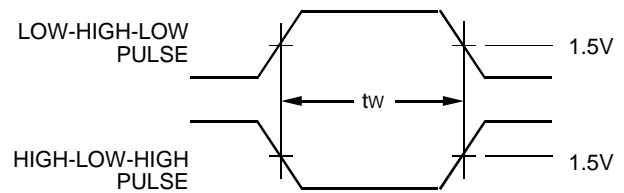
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

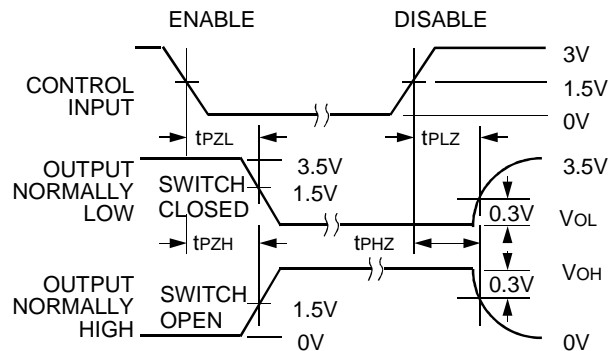
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

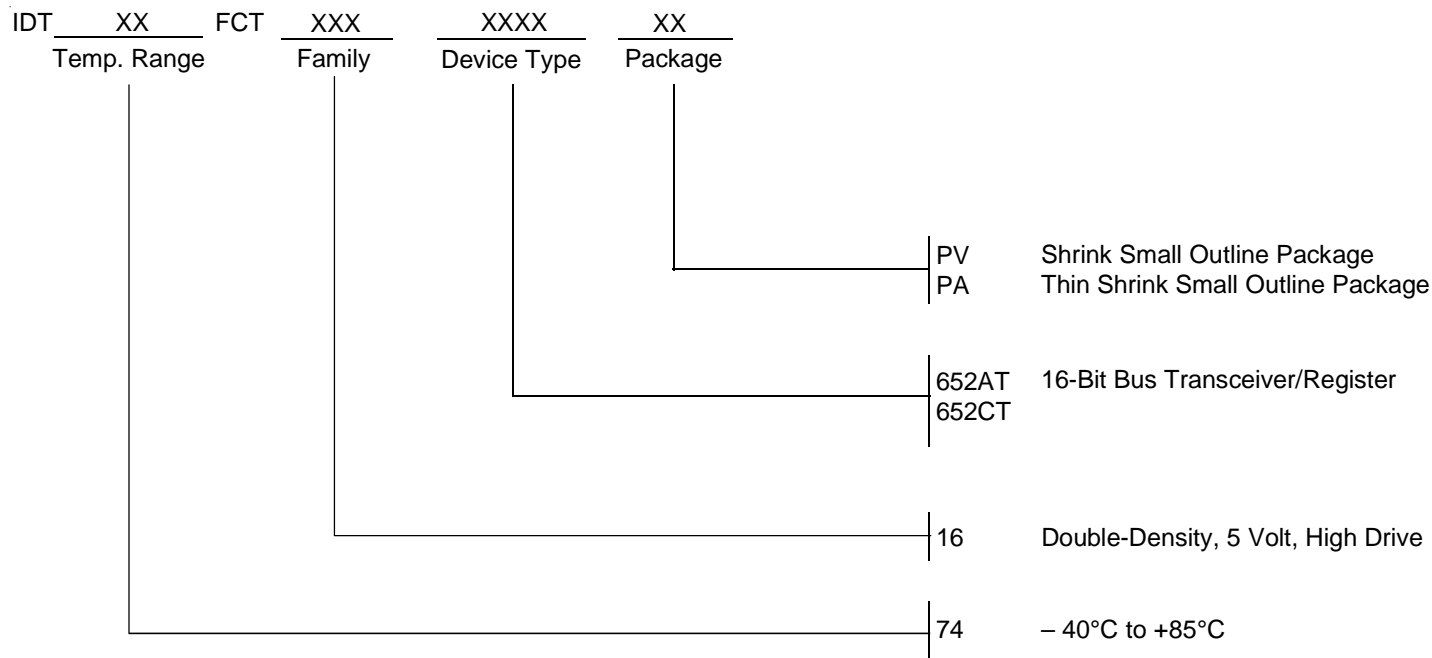


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_r \leq$ 2.5ns; $t_f \leq$ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

1/21/2002 Removed Military temp grade
6/21/2002 Updated as per PDNs Logic-00-07 and Logic-01-04



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